

IN THE CLAIMS

1 1. (Currently Amended) A method for designing a system on a target device utilizing
2 field programmable gate arrays (FPGAs), comprising:
3 identifying a group of components associated with a critical signal in the system;
4 creating a first copy and a second copy of the group of components where the first copy
5 is driven by a first signal at a first state and the second copy is driven by a second signal at a
6 second state; and
7 configuring the system to utilize a selector circuit on the target device to select an output
8 of one of the first copy and the second copy in response to the critical signal.

1 2. (Original) The method of Claim 1, wherein identifying the group of components
2 associated with the critical signal in the system comprises determining a transitive fanout for the
3 critical signal.

1 3. (Original) The method of Claim 2, wherein determining the transitive fanout for the
2 critical signal comprises identifying the transitive fanout within a maximum number of logic
3 levels.

1 4. (Original) The method of Claim 2, further comprising:
2 identifying side inputs to the transitive fanout; and
3 determining whether the side inputs have sufficient slack.

1 5. (Original) The method of Claim 1, further comprising providing connections from
2 side inputs in the system to components in each of the first copy and second copy.

1 6. (Original) The method of Claim 1, further comprising removing unused components
2 from the group of components.

1 7. (Original) The method of Claim 1, further comprising determining the critical signal
2 by performing a critical path traceback procedure.

1 8. (Currently Amended) The method of Claim 1, further comprising determining
2 appropriate placement of the first copy and the second copy on the target device using an
3 incremental placement technique to resolve illegalities in placement by moving components not
4 associated with the critical signal to allow the first copy and the second copy to be placed at
5 preferred locations.

1 9. (Original) The method of Claim 2, further comprising:
2 determining a transitive fanout for a signal identified as being next most critical for the
3 system;
4 creating a first copy and second copy of a group of components associated with the
5 transitive fanout for the signal identified as being next most critical for the system; and
6 configuring the system to select an output of one of the first copy and the second copy of
7 the group of components associated with the transitive fanout in response to the signal identified
8 as being next most critical for the system.

1 Claims 10-25 (Canceled)

1 26. (Currently Amended) A machine-readable medium having stored thereon sequences
2 of instructions, the sequences of instructions including instructions which, when executed by a
3 processor, causes the processor to perform:

4 identifying a group of components associated with a critical signal in a system;
5 creating a first copy and a second copy of the group of components where the first copy
6 is driven by a first signal at a first state and the second copy is driven by a second signal at a
7 second state; and
8 configuring the system to utilize a selector circuit to select an output of one of the first
9 copy and the second copy in response to the critical signal.

1 27. (Previously Presented) The machine-readable medium of Claim 26, wherein
2 identifying the group of components associated with the critical signal in the system comprises
3 determining a transitive fanout for the critical signal.

1 28. (Previously Presented) The machine-readable medium of Claim 26, wherein
2 determining the transitive fanout for the critical signal comprises identifying the transitive fanout
3 within a maximum number of logic levels.

1 29. (Previously Presented) The machine-readable medium of Claim 27, further
2 comprising instructions which when executed causes the processor to perform:
3 identifying side inputs to the transitive fanout; and
4 determining whether the side inputs have sufficient slack.

1 30. (Previously Presented) The machine-readable medium of Claim 26, further
2 comprising instructions which when executed causes the processor to perform providing
3 connections from side inputs in the system to components in each of the first copy and second
4 copy.

1 31. (Previously Presented) The machine-readable medium of Claim 26, further
2 comprising instructions which when executed causes the processor to perform removing unused
3 components from the group of components.

1 32. (Previously Presented) The machine-readable medium of Claim 26, further
2 comprising instructions which when executed causes the processor to perform determining the
3 critical signal by performing a critical path traceback procedure.

1 33. (Currently Amended) The machine-readable medium of Claim 26, further
2 comprising instructions which when executed causes the processor to perform determining
3 appropriate placement of the first copy and the second copy on the target device using an
4 incremental placement technique to resolve illegalities in placement by moving components not
5 associated with the critical signal to allow the first copy and the second copy to be placed at
6 preferred locations.

1 34. (Previously Presented) The machine-readable medium of Claim 27, further
2 comprising instructions which when executed causes the processor to perform:
3 determining a transitive fanout for a signal identified as being next most critical for the
4 system;
5 creating a first copy and second copy of a group of components associated with the
6 transitive fanout for the signal identified as being next most critical for the system; and
7 configuring the system to select an output of one of the first copy and the second copy of
8 the group of components associated with the transitive fanout in response to the signal identified
9 as being next most critical for the system.

1 35. (Previously Presented) An electronic design automation (EDA) tool, comprising:

2 a layout-driven optimization engine to identify a group of components associated with a
3 critical signal in a system, create a first copy and a second copy of the group of components
4 where the first copy is driven by a first signal at a first state and the second copy is driven by a
5 second signal at a second state, and configure the system to utilize a selector circuit to select an
6 output of one of the first copy and the second copy in response to the critical signal.

1 36. (Currently Amended) The EDA tool of Claim 35, further comprising an incremental
2 placement engine to determine an appropriate placement of the first copy and the second copy on
3 the target device using an incremental placement technique to resolve illegalities in placement by
4 moving components not associated with the critical signal to allow the first copy and the second
5 copy to be placed at preferred locations.